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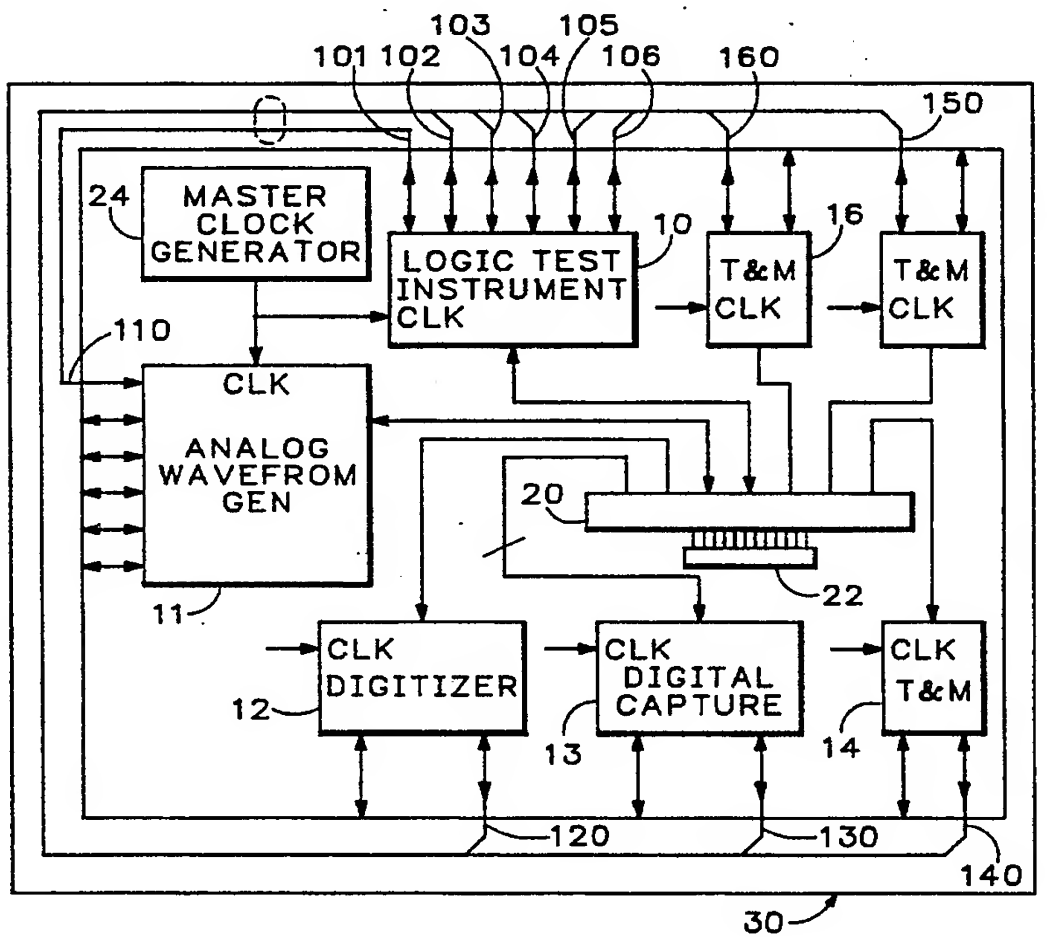
(54) Title: APPARATUS FOR AUTOMATIC TESTING OF COMPLEX DEVICES

(57) Abstract

Apparatus for testing an integrated circuit device (DUT) having an input port and an output port comprises multiple state devices (10-16) each having multiple states that occur in a predetermined sequence and an output port at which it provides an event signal. A first of the state device is an emitting device (10) that emits an event marker signal at a predetermined time in advance of entering a predefined state, a second of the state devices is a receiving device (11) that responds to receipt of an event marker signal, at least one of the state devices (11) has its output port connected to the input port of the DUT, and at least one of the state devices is a measurement device (13) connected to the output port of the DUT. An interconnection matrix (30) is connected to each state device and allows each state device to communicate an event marker signal to each other.



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APPARATUS FOR AUTOMATIC TESTING OF COMPLEX DEVICES

Background of the Invention

This invention relates to apparatus for automatic testing of complex devices, and is particularly applicable to apparatus for automatic testing of complex electronic circuit devices. Such devices may be fabricated in a variety of technologies and over a wide range of integration scales.

In manufacture of electronic circuit devices, it is important to be able to verify that a particular unit meets the functional specifications prescribed for that model of circuit. Such an electronic circuit device is typically tested either manually, with discrete test and measurement instruments, or by using an automated test equipment (ATE) system if one with sufficient capability is available. Use of an automated test system is preferred over the manual method of testing for reasons of speed, accuracy and repeatability, but an automated test system often cannot provide adequate capabilities to perform all required tests for full and accurate device parameter verification.

An ATE system comprises a test socket that is mated with connection pins of the device under test (DUT), a stimulus device for applying a preset sequence of stimuli to the DUT and an acquisition device for receiving signals representative of the response of the DUT to the stimuli. Computer control of stimulus and acquisition instrumentation resources integrate the whole into a system that is instructed through software to perform complex testing processes.

In a conventional ATE system, the stimulus device and the acquisition device operate under timing control of a single master event controlling device which specifies the phase relationships between all activities in a given test procedure. In order to provide maximum accuracy while also providing minimum test time, Digital Signal Processing (DSP) techniques are employed for testing of analog parameters and relationships between analog (continuously variable) and digital (discretely variable) activities. The primary requirement for rapidly-executing DSP test techniques is coherent timing between stimulus and acquisition activities. Coherent timing requires precise integer ratios between frequencies of execution and renders absolute accuracy of the frequencies of much less importance. For this reason, a conventional coherent automated test system contains a single master timing reference from which all stimulus and acquisition device state timing is derived.

This timing approach allows many characteristics of the DUT to be measured, but is subject to some limitations. For example, the conventional coherent ATE system, having a single master event controlling device, is not well suited to testing certain device parameters. For example, an important figure-of-merit relative to an analog-to-digital converter (ADC) is the linearity of the quantization process utilized for the conversion of a continuously-variable analog signal to discrete values in an evenly spaced digital scale. The conversion linearity depends on the accuracy of the sampler portion of the ADC. Certain high-speed samplers employ a circuit

configuration that is not stable for more than a short period of time after being placed into a known stable calibration state and released for operation. Such a sampler therefore requires repeated calibration. The ADC is placed in its calibration state by a discrete stimulus signal from an external source, typically a micro-controller that is controlling operation of the apparatus containing the ADC. Although the ADC is continuously sampling and producing output data, the output data produced during a calibration cycle is invalid. An ADC with an unstable sampler of this type exhibits an overall operating cycle composed of a calibration cycle followed by a conversion cycle, which may contain multiple sampling and quantizing cycles.

The conversion linearity of an ADC with an unstable sampler may depend on the duration of the calibration cycle and the interval between calibration cycles. This implies that in order to measure conversion linearity of such an ADC, the tester must include stimulus and acquisition devices that operate intermittently. The requirement of coherent timing forces the stimulus, acquisition and controlling devices of the ATE system to operate at differing frequencies of state alteration as their respective tasks are executed. This creates great difficulty for a single event master device to accurately control starting, stopping, pausing and resumption of the various device activities as a test procedure executes.

Unstable configuration ADC sampling circuits are typically employed in applications intended for very high speed operation with many bits of resolution, such as high performance video graphics

for computer-aided design tools. The combination of both high conversion rate and fine resolution implies that a large amount of data must be acquired in order to provide sufficient data points to adequately measure parameters to an accuracy corresponding to that resolution. The required number of data points cannot be acquired at the operating rate of the ADC in the maximum period of time available between successive calibration cycles. Therefore, the test process is forced to be discontinuous, with data gathered over multiple active periods between calibration cycles.

Ideally, the acquisition device captures only data generated by the ADC under test during active periods between calibration cycles. Additionally, the resulting data record is ideally a single, continuous set of all data points with no redundancy and a seamless continuity so that subsequent DSP data reduction algorithms are simple and rapidly executing. This would require that the test process be interrupted and resumed in response to the periodic calibration cycles so that the resulting data record appears to be a single continuous acquisition.

A conventional ATE system exhibits difficulty in management of the phase between measurement discontinuities among the separate test resource devices so that an extended acquisition period is required to ensure that all data is captured through redundancy over a number of active periods of the ADC under test. As a result, it is necessary to eliminate from the data record any data acquired while the ADC was undergoing calibration, and this can lead to difficulty in accurately and rapidly measuring such parameters as the linearity of the

conversion process due to extensive pre-processing of the data record before the ideal seamless, complete-without-redundancy data record is produced.

Further, the conventional ATE system is not well suited to testing of a more general set of devices composed of functional blocks that operate in different time domains. The ADC discussed above embodies at least three time domains (the analog input sourcing device, the digital controlling device and the digital output acquisition device). A typical video processing circuit might include an ADC that operates under control of a synchronization signal associated with the analog input, a digital processing circuit connected to a standard digital interface and a digital-to-analog converter (DAC) producing an analog representation of the processed input signal for output in accordance with a video display standard. The establishment of the specific timing requirements of these different time domains leads to difficulty in testing characteristics that involve more than one functional block.

Summary of the Invention

In accordance with the present invention there is provided an apparatus for testing a complex device under test (DUT) having an input port and an output port, said apparatus comprising a plurality of state devices each having multiple states that occur in a predetermined sequence and each having an output port at which it provides an event signal representative of its current state, at least a first of the state devices being an emitting device that emits an event marker signal at a predetermined time in advance of entering a predefined state, at least a second of the state devices being a

receiving device that responds to receipt of an event marker signal in a predetermined manner after lapse of a predetermined time, at least one of the state devices having its output port connected to the input port of the DUT, and at least one of the state devices being a measurement device connected to the output port of the DUT. The apparatus also comprises an interconnection matrix connected to each state device and allowing each state device to communicate an event marker signal to each other state device.

Brief Description of the Drawings

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings in which:

FIG. 1 is a block diagram of apparatus in accordance with the present invention;

FIG. 2 illustrates in greater detail a component of the apparatus shown in FIG. 1;

FIG. 3 is a graph illustrating use of the apparatus shown in FIGS. 1 and 2 to carry out a discontinuous linearity test on an unstable configuration analog-to-digital converter; and

FIG. 4 is a graph illustrating use of the apparatus shown in FIGS. 1 and 2 to carry out a further test on an unstable configuration analog-to-digital canister.

Detailed Description

The tester shown in FIG. 1 comprises multiple quasi-independent state machines 10-16, including a logic test instrument 10 and test and measurement (T & M) instruments 11-16. The state machines

10-16 are each connected through a socket 20 to a device under test 22. The state machines 10-16 may have single line socket connection ports or multiple line socket connection ports, depending on the nature of the state machine, the nature of the DUT and the nature of the test that is to be carried out. The socket 20 may have upwards of one hundred pins, although some pins might not be used for a particular test. The different state machines 10-16 are at different distances from the socket, and accordingly the signal propagation time between the socket and the state machine is not uniform over all state machines.

The logic test instrument is an autonomous instrument having substantially all the functions of a conventional digital tester. Thus, the logic test instrument is able to generate a digital stimulus signal and to receive and measure a digital response signal. Some conventional digital testers might have capabilities that go beyond what is necessary for the logic test instrument. For example, the logic test instrument might be one of the Vista series testers sold by Credence Systems Corporation of Fremont, California.

The T & M instruments 11-16 are autonomous instruments, each dedicated to a particular T & M function. For example, the T & M instruments might include an analog waveform generator 11, an analog waveform digitizer 12, a digital capture port 13, and other instruments 14, 15, 16. Each of the T & M instruments has an active state and quiescent state. The analog waveform generator supplies an analog output signal to the DUT. In the active state of the analog waveform generator, the analog output signal varies in accordance with a

user-selected waveform, e.g. a stair step waveform or a sinusoidal waveform, and in the quiescent state, the output signal remains at a constant level. When the analog waveform digitizer is in use, it receives an analog output signal from the DUT. In its active state, the analog waveform digitizer converts the analog signal from the DUT to digital form, and in its quiescent state the digitizer interrupts conversion of the analog signal to digital form. When the digital capture port is in use, the digital capture port receives a digital output signal from the DUT. In its active state, the digital capture port generates acquisition strobe pulses in order to acquire the digital output signal of the DUT, and in the quiescent state the digital capture port interrupts generation of acquisition strobe pulses.

The tester also includes an interconnection matrix 30 whereby the state machines 10-16 are connected to each other in a manner that allows simultaneous bidirectional communication between each two state machines. Thus, the matrix has bidirectional communication ports 101-106 that are connected to the logic test instrument 10 and ports 110, 120, 130, 140, 150 and 160 that are connected through the matrix to the ports 101-106 respectively and are also connected to the T & M instruments 11-16 respectively for providing communication between the logic test instrument 10 and each of the T & M instruments 11-16. Additional ports (not shown) provide communication between each other pair of state machines.

The state machines 10-16 all operate under control of a master clock that is generated by a master clock generator 24. Clock lines extend from

the master clock generator 24 to each of the state machines 10-16. Each state machine has an internal timing generator (not shown) that operates in response to the master clock and generates a local clock at a frequency that is related to the frequency of the master clock by a predetermined integer ratio that is not necessarily the same as the integer ratio that relates the local clock frequency of any other state machine to the master clock frequency. Therefore, all the local clocks are coherent and remain coherent even if the frequency of the master clock changes. Different integer ratios allow different rates of state progression in the different state machines. In response to its internal time domain, the logic test instrument 10 steps through a progression of states that depends on the particular test that is to be executed. Similarly, each T & M instrument 11-16 that is used for a particular test operates in its own internal time domain and steps through a progression of states that depends on commands applied to the instrument by the logic test instrument 10.

FIG. 2 illustrates in somewhat greater detail the interface between the logic test instrument 10 and the matrix 30. The port 101 comprises a marker generator 36 connected to an output line of the logic test instrument 10. The output line might be the output of one of the pin channels of the logic test instrument. For certain states of the logic test instrument, there are precursor states that occur in advance and result in a signal being provided to the marker generator 36. In response to this signal, the marker generator 36 provides a marker signal to the analog waveform generator 11 by way of a dedicated line 38 and the port 110

(FIG. 1). The marker signal is received at the port 110 at a precisely defined time in advance of occurrence of the state that is anticipated by the precursor state. The port 101 also includes a marker detector 40 that detects a marker received from the analog waveform generator by way of the port 110 and a dedicated line 42. A controllable delay element 44 is interposed between the marker detector 40 and the logic test instrument 10, so that the logic test instrument receives a signal indicating that a marker from the analog waveform generator has been detected at a controllable time after detection of the marker. Each of the other bidirectional communication ports of the matrix 30 is similarly equipped with a marker generator, a marker receiver and a controllable delay element. Thus, the marker signal received at the port 110 is subject to a precisely defined delay before being received by the analog waveform generator.

Not all T & M instruments are used in carrying out a given test. For example, in order to test conversion linearity of an ADC using the tester shown in FIGS. 1 and 2, the tester is configured to use the logic test instrument 10, the analog waveform generator 11 and the digital capture port 13. The logic test instrument 10, the analog waveform generator 11 and the digital capture port 13 each execute a predetermined sequence of steps.

In order to test conversion linearity of an ADC, the analog waveform generator may be programmed to generate a stairstep waveform under control of its local clock. In setting up the test, the operator decides on the duration and frequency of the calibration cycles of the ADC, and programs the logic test instrument to emit periodically a

discrete reset pulse (ADC zero - FIG. 3, waveform F), which is applied to the reset pin of the ADC through the socket 20, at a selected time relative to the master clock. Therefore, the logic test instrument 10 periodically causes the ADC to execute a calibration cycle of a selected duration. The operator also programs the logic test instrument to emit a vector trigger start pulse 50 (waveform E) just before the start of each conversion cycle and a vector trigger stop pulse 52 just before the end of each conversion cycle. The vector trigger signal is applied to the port 101 of the interconnection matrix. The port 101 responds to the vector trigger signal by generating an LT trigger 1 signal (waveform B) that is applied to the port 110. The LT trigger 1 signal is delayed relative to the vector trigger signal to ensure that it is received by the analog waveform generator at an accurately repeatable time in advance of entry of the logic test instrument into the anticipated state, i.e. the state in which the ADC zero pulse ends.

The port 110 of the matrix 30 responds to the LT trigger 1 signal by delaying it for a predetermined time and applying the delayed LT trigger 1 signal to the analog waveform generator 11. The analog waveform generator responds to a delayed LT trigger 1 start pulse 50' by entering its active state, so that on the next pulse of the local clock the output voltage of the analog waveform generator increases by one increment. The analog waveform generator responds to a delayed LT trigger 1 stop pulse 52' by entering its quiescent state, so that the increment in output voltage on the next local clock pulse is the last until the next start pulse 50' is received. Therefore, the

output voltage of the analog waveform generator increases in an intermittent, stepwise fashion under control of the LT trigger 1 pulses. The intermittent stepwise increasing of the output voltage of the analog waveform generator continues within the range of the output voltage of the analog waveform generator.

The vector trigger pulses are also applied to the port 103 of the interconnection matrix. The port 103 responds to the vector trigger signal by generating an LT trigger 2 signal that is applied to the port 130. (Although waveform B in FIG. 3 is indicated as representing both the LT trigger 1 signal and the LT trigger 2 signal, the two signals would generally be offset in time relative to each other.) The port 130 of the matrix responds to the LT trigger 2 signal by supplying a delayed LT trigger 2 signal to the digital capture port 13. The digital capture port 13 is connected to the digital output pins of the ADC 22 and acquires the digital output signal of the ADC for analysis relative to the state of the analog waveform generator. The digital capture port responds to a delayed LT trigger 2 start pulse by entering its active state, so that on the next pulse of the local clock the digital capture port commences generating periodic acquisition strobe pulses (waveform D). The digital capture port responds to a delayed LT trigger 2 stop pulse by entering its quiescent state, so that the strobe pulse generated on the next local clock pulse is the last until the next LT trigger 2 start pulse is received.

The delay elements of the bidirectional communication ports are calibrated so that the predetermined time that elapses between receipt of

a marker, such as the delayed LT trigger 1 start pulse, and the resulting change in state of the state machine that received the delayed marker is such that the change in state of the state machine occurs at a selected time relative to the change in state that is anticipated by the marker. For example, in order to acquire valid data for the discontinuous conversion linearity test, the predetermined times that control entry of the analog waveform generator and the digital capture port into the active states must be such that when the digital capture port generates an acquisition strobe pulse, the ADC is executing a conversion cycle and the analog waveform generator is in its active state. These times are determined by connecting a calibration device to the socket 20 in lieu of the ADC 22. The calibration device may be the autocalibration system sold by Credence Systems Corporation as an option to its Vista series testers. In order to determine the proper delay for the analog waveform generator, the calibration device detects arrival at the socket 20 of both the change of state indicating start of the conversion cycle (falling edge of ADC zero) and the stepwise increase in the output voltage of the analog waveform generator for various settings of the delay element in the port 110, and the delay imposed by the delay element of the port 110 is selected such as to provide the desired relationship. Similarly, in order to determine the proper time delay for the digital capture port, the calibration device emits a pulse signal to the digital capture port by way of the socket 20 and for various values of the delay element in the port 130 a determination is made as to whether the leading edge of the pulse

signal has been acquired by the capture port. The delay imposed by the delay element is selected so that the leading edge of the pulse signal is acquired.

It will therefore be seen that use of the tester described with reference to FIGS. 1 and 2 allows operation of the analog waveform generator and digital capture port to be controlled relative to the state of the logic test instrument 10, as manifested by the vector trigger signal, rather than simply in response to passage of time, as in a timing driven tester.

Another figure of merit relevant to an ADC can be derived from analysis of data values acquired in response to a sinusoidal stimulus signal. The Fast Fourier transform (FFT) algorithm allows rapid analysis of a data record representative of a periodic waveform provided that the record contains 2**n, where n is an integer, data points spanning precisely an integer number of cycles of the periodic waveform. In the case of an ADC with an unstable sampler, it is impossible to acquire sufficient data between two consecutive calibration cycles. The apparatus shown in FIGS. 1 and 2 may be used to acquire a data record in several segments distributed over multiple cycles of the sinusoidal stimulus signal without corrupting the record with a large volume of spurious data.

In order to carry out this test, the analog waveform generator is programmed to generate voltage samples at a high frequency by stepping through a progression of states in response to its local clock, the samples being related in accordance with a sinusoidal function of time. The sampled signal is low-pass filtered, and the

resulting continuous analog output signal (FIG. 4, waveform B) is applied to the DUT. The operator determines how many cycles of the sinusoidal waveform should be acquired, and the record length, i.e. the number of samples that should be taken.

As shown in FIG. 4, the ADC zero signal emitted by the logic test instrument periodically includes a pulse that places the ADC in its active state. In anticipation of entry into the active state of the ADC, the logic test instrument generates a vector trigger signal, which it applies to the ports 101 and 103. The ports 101 and 103 emit an LT trigger 1 signal and an LT trigger 2 signal (waveform C) respectively, each with a predetermined delay following the vector trigger signal. As in the case of FIG. 3, the two LT trigger signals will not generally be in phase. The LT trigger 1 signal is applied to the analog waveform generator and the LT trigger 2 signal is applied to the digital capture port. In response to the first LT trigger 2 start pulse, the digital capture port generates acquisition strobe pulses, for capturing the digital output of the ADC. In response to the first LT trigger 1 stop pulse, the analog waveform generator stores the count representative of its state at a predetermined later time, and in response to the first LT trigger 2 stop pulse the digital capture port stops generating acquisition strobe pulses. The aforesaid predetermined later time is such that the count stored by the analog waveform generator corresponds to the end of the acquisition made by the digital capture port.

On subsequent cycles of the sinusoidal output, the analog waveform generator generates an AWG trigger pulse (waveform A) in advance of the

time that the analog waveform generator reaches the state represented by the count stored in response to the first LT trigger 1 stop pulse, and the AWG trigger pulse is applied over the interconnection matrix 30 to the digital capture port. Moreover, the second LT trigger 2 start pulse does not cause the digital capture port to generate acquisition strobe pulses but rather arms the digital capture port so that on receiving the delayed AWG trigger pulse, the digital capture port will resume generation of acquisition strobe pulses and will capture the output signal of the ADC resulting from sampling and quantizing a segment of the cycle of the analog waveform that immediately follows the segment that was sampled and quantized during the preceding succession of acquisition strobe pulses. In response to the second LT trigger 2 stop pulse, the digital capture port stops generating acquisition strobe pulses, and in response to the second LT trigger 1 stop pulse the analog waveform generator stores the count representative of its state at the predetermined later time. This sequence of operation continues until the digital capture port has acquired a complete record for analysis.

The tester shown in FIGS. 1 and 2 may also be used to test a more complex device, such as one that includes both an ADC and a circuit for digital processing of the output of the ADC. In testing such a device, the logic test instrument 10 of the tester is connected to a digital control port of the digital processing circuit and the digital capture port is connected to the output of the digital processing circuit. The logic test instrument 10 might, for example, examine the signals provided at the digital control port in order to ascertain

whether the digital processing circuit has determined that the output of the ADC is stable, so that a particular action can be invoked.

In the test described with reference to FIG. 3, the logic test instrument is the master instrument and the analog waveform generator and digital capture port are slave instruments, whereas in the case of the test described with reference to FIG. 4, the analog waveform generator functions as a master instrument. It will therefore be seen that the illustrated tester has the ability to alter the nature of master-slave timing relationships between ATE system instruments.

The different instruments within the test system execute with independently specifiable timing of state alterations. Time correlation between particular states-of-interest found within these separately executing state progressions are established arbitrarily.

It will be appreciated that the invention is not restricted to the particular embodiment that has been described, and that variations may be made therein without departing from the scope of the invention as defined in the appended claims and equivalents thereof. For example, the invention is not restricted to apparatus for testing monolithic integrated circuits but is also applicable to testing of hybrid integrated circuits and multiple integrated circuits mounted on a circuit board. Furthermore, the invention is not restricted to the testing of electronic devices, since with suitable stimulus and acquisition instruments it may also be applied to integrated optic devices.

The test described with reference to FIG. 4 shows that the apparatus shown in FIGS. 1 and 2 is

not restricted to each T & M instrument operating as a slave relative to the logic test instrument. In the case of the test described with reference to FIG. 4, the analog waveform generator itself serves as a master instrument controlling operation of the digital capture port.

Since each of the instruments is autonomous and each slave instrument executes its progression of states in response to an event marker, the time of occurrence of the event marker does not affect operation of the slave instrument. On receipt of the event marker, the slave instrument executes its progression of states without regard to operation of the master instrument or any other slave instrument, unless it receives another event marker.

For the purpose of this invention, a state is characterized by a period of time during which one or more events may occur, and an event characterizes a point-in-time at which other events may be caused to occur.

It will be appreciated that it is necessary that the local clock generators be capable of controlling accurately the delay between receiving a delayed event marker and the response to the delayed marker, and that the position of the LT trigger stop pulse be controlled very accurately so that it arrives between two clocks of the analog waveform generator or digital capture port and there is no ambiguity over which clock of the analog waveform generator or digital capture port is the next (and last) pulse in the active cycle. It is relatively easy to control the start of generation of acquisition strobe pulses relative to receipt of the LT trigger 2 start pulse, but it is much more difficult to control accurately the time to discontinue generation of acquisition strobe pulses relative to the LT trigger

2 start pulse, and therefore ending of the operation of generating acquisition strobe pulses is controlled by the LT trigger 2 stop pulse.

Claims

1. Apparatus for testing an integrated circuit device (DUT) having an input port and an output port, said apparatus comprising:

a plurality of state devices (10-16) each having multiple states that occur in a predetermined sequence and each having an output port at which it provides an event signal representative of its current state, at least a first of the state devices being an emitting device (10) that emits an event marker signal at a predetermined time in advance of entering a predefined state, at least a second of the state devices being a receiving device (11) that responds to receipt of an event marker signal in a predetermined manner after lapse of a predetermined time, at least one of the state devices (11) having its output port connected to the input port of the DUT, and at least one of the state devices being a measurement device (13) connected to the output port of the DUT, and

an interconnection matrix (30) connected to each state device and allowing each state device to communicate an event marker signal to each other state device.

2. Apparatus according to claim 1, wherein the interconnection matrix (30) comprises a plurality of bidirectional communication ports connected to each state machine for allowing communication between each two state machines, and wherein each bidirectional communication port comprises a marker signal generator (36) connected to the state machine for emitting a marker signal

in response to a signal received from the state machine, a marker signal detector (40) connected to receive a marker signal from the matrix and to generate a signal in response thereto, and a controllable delay element (44) connected between the marker signal detector and the state machine.

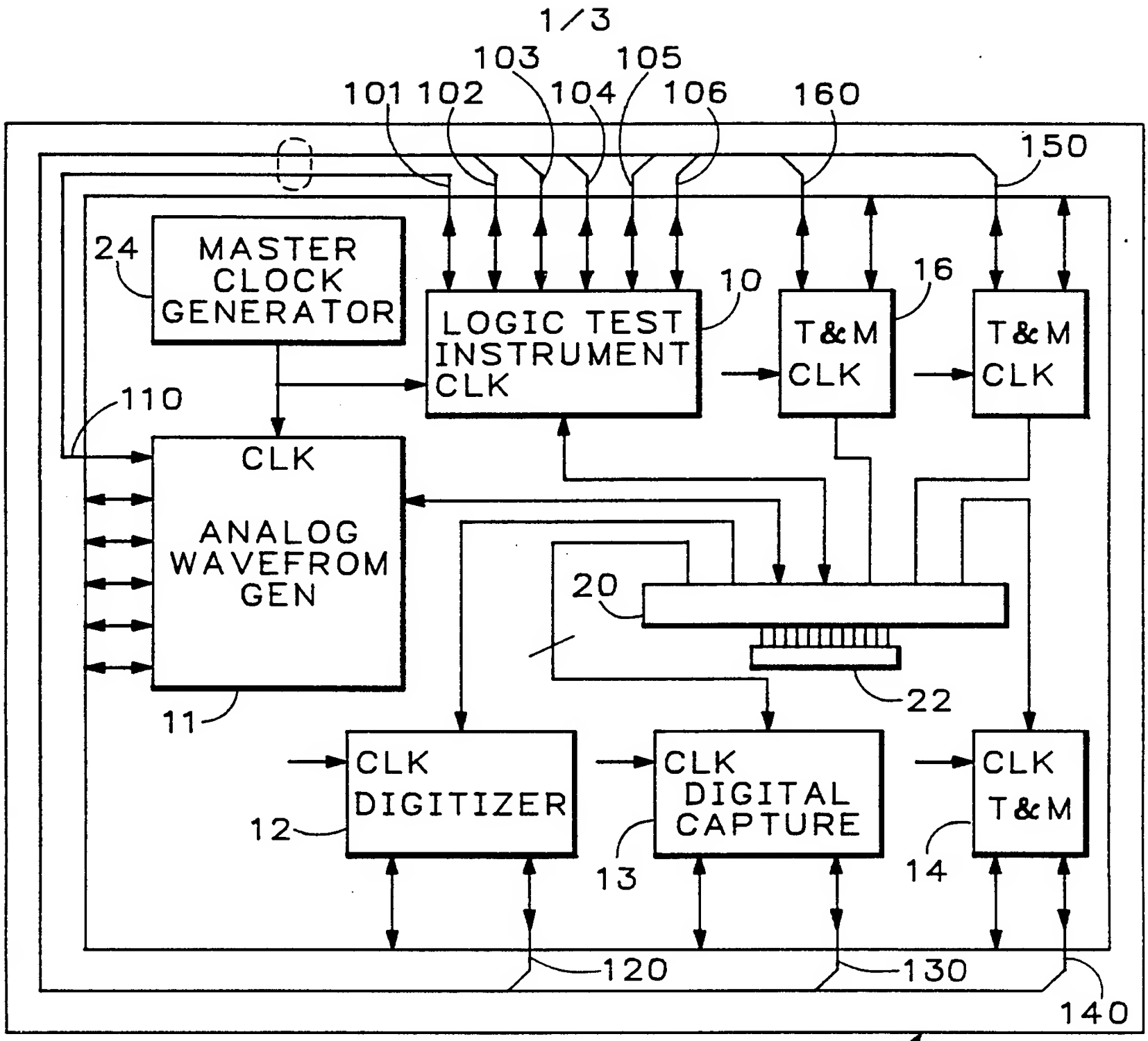
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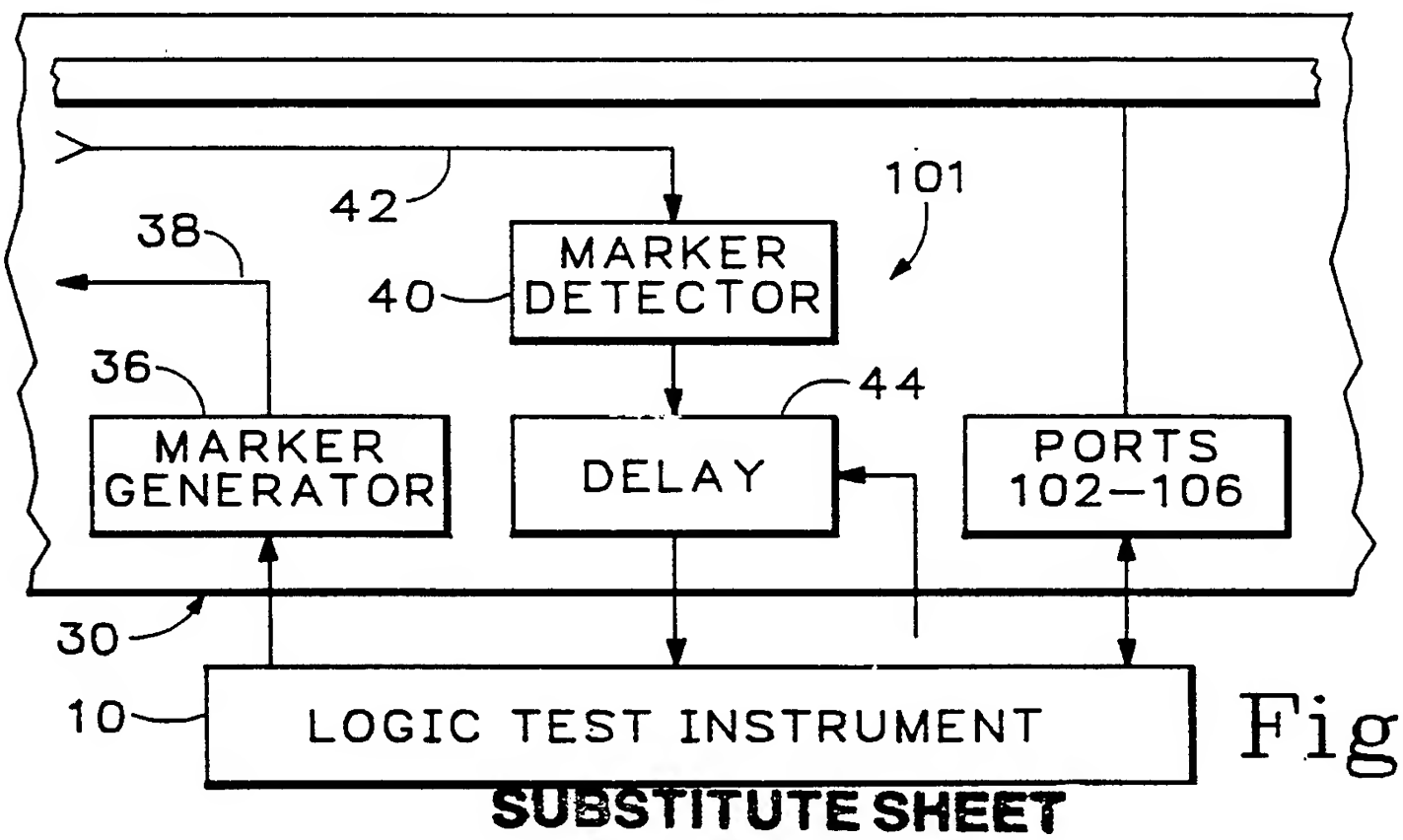
Fig.1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MARKER DETECTOR
40
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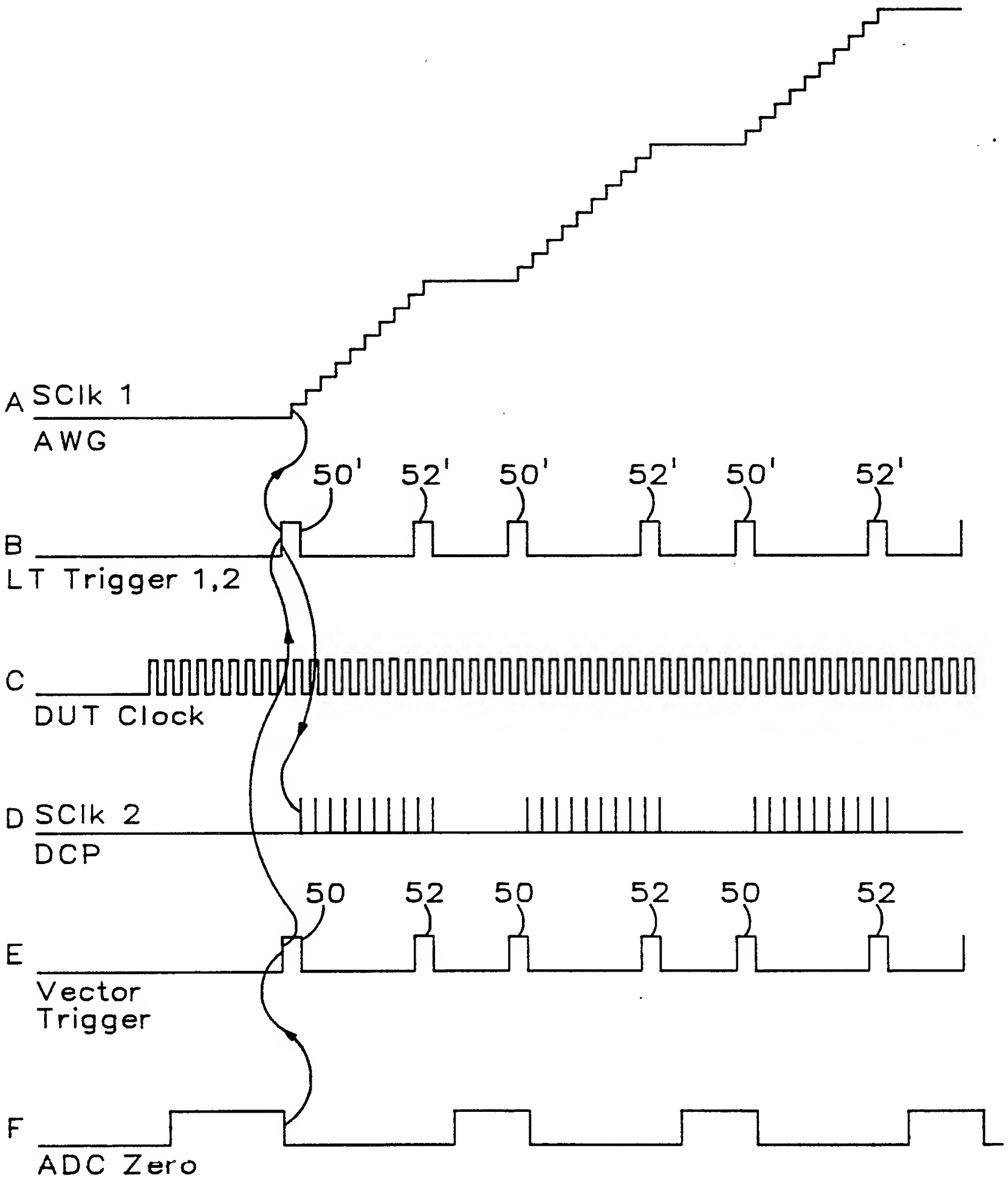
MARKER GENERATOR
DELAY
PORTS 102–106
30
10
LOGIC TEST INSTRUMENT

Fig.2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LT Trigger 1,2
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50
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Vector
Trigger
F
ADC Zero

Fig. 3

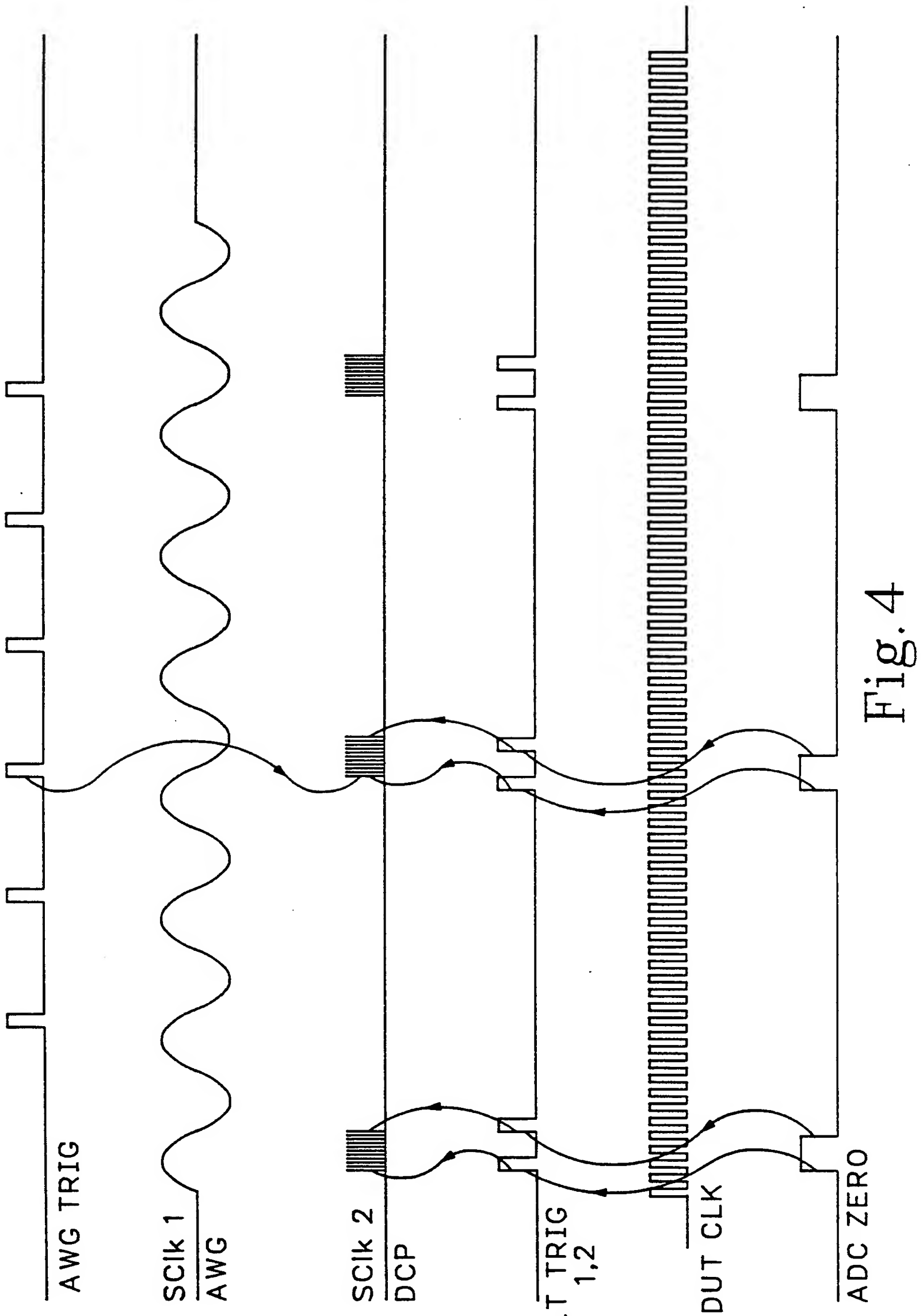

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/07020

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :G01R 31/28
US CL :324/158R, 73.1, 371/15.1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

US CL.: 324/158R, 73.1/371/15.1 368/113; 371/22.1, 22.3, 22.6, 25.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

none

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A 4,544,882 (FLORA) 01 OCTOBER 1985 (see figure 1, the abstract and entire document)	1
X	US, A, 4,816,750 (VAN DER KLOOT ET AL) 08 MARCH 1989 (see figure #1 and entire document)	1
A	US, A, 4,835,459 (HAMLIN ET AL) 30 MAY 1989 (see figure 1 and the abstract)	1-2
A	US, A, 5,126,953 (BERGER ET AL) 30 JUNE 1992 (see figure 1 and the abstract)	1-2

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 02 SEPTEMBER 1993	Date of mailing of the international search report 25 OCT 1993
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer VINH P. NGUYEN Telephone No. (703) 305-4914

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